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without limits.

3D ICs: Recent Advances in the Industry

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Senior Director, Advanced Packaging

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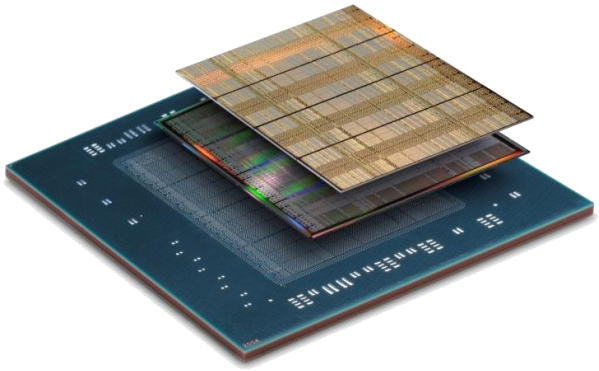
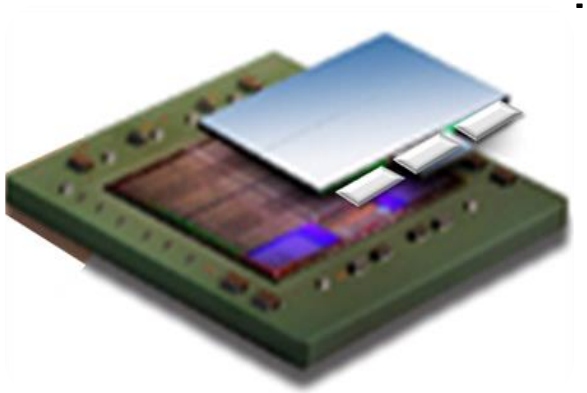
Outline

- 3D IC Background
- 3D IC Technology Development
- Summary
- Acknowledgements

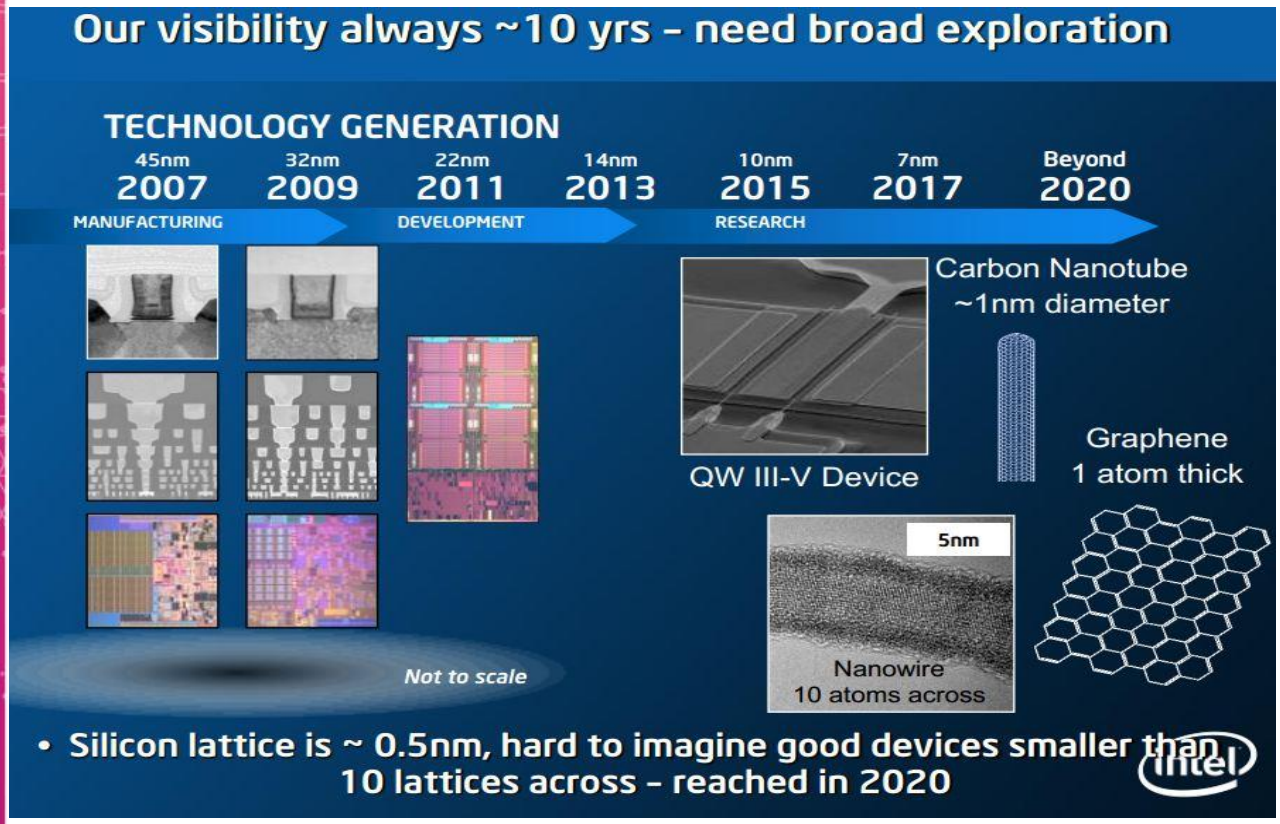




Stacked ***S***ilicon ***I***nterconnect ***T***echnology Refers to Xilinx 3D solutions

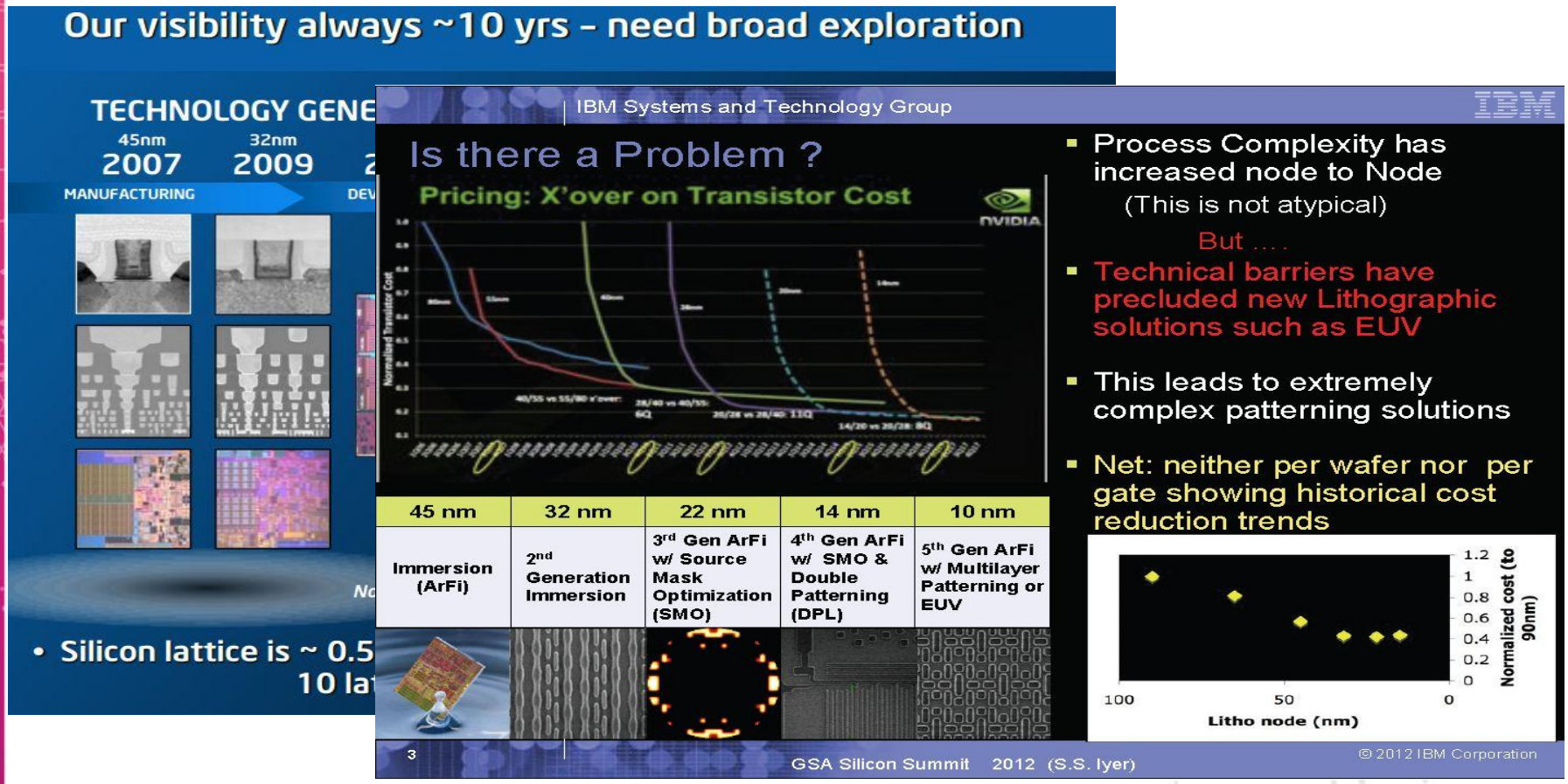
3D IC Background

Technical Challenges & Costs Are Growing



- Process Technology Path Below 7nm is unclear
- Cost Reduction Slowing from Complexity / Investment Increases
- Cost Per Wafer & Cost Per Gate Deviating from Historical Reduction

Technical Challenges & Costs Are Growing



- Process Technology Path Below 7nm is unclear
- Cost Reduction Slowing from Complexity / Investment Increases
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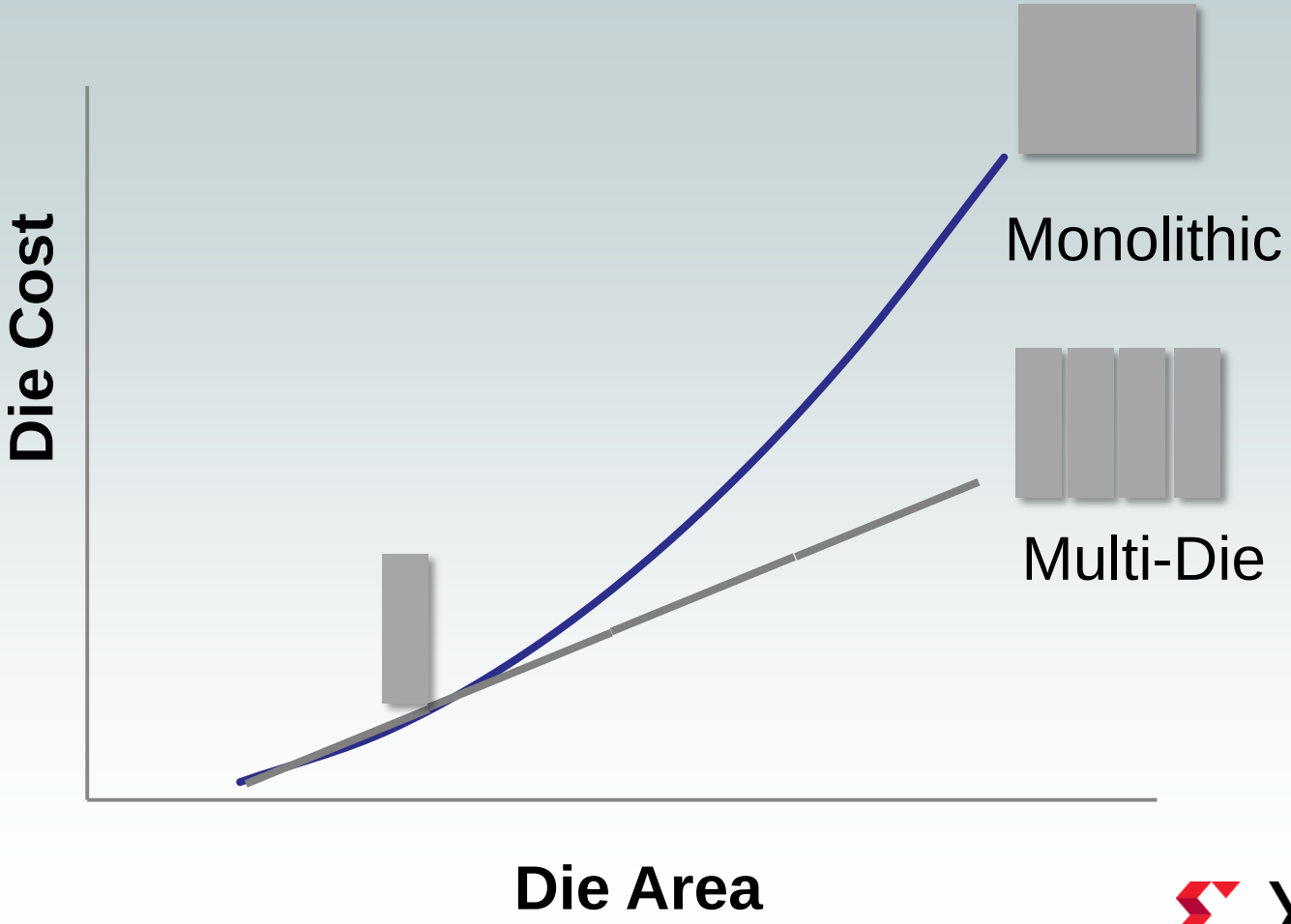
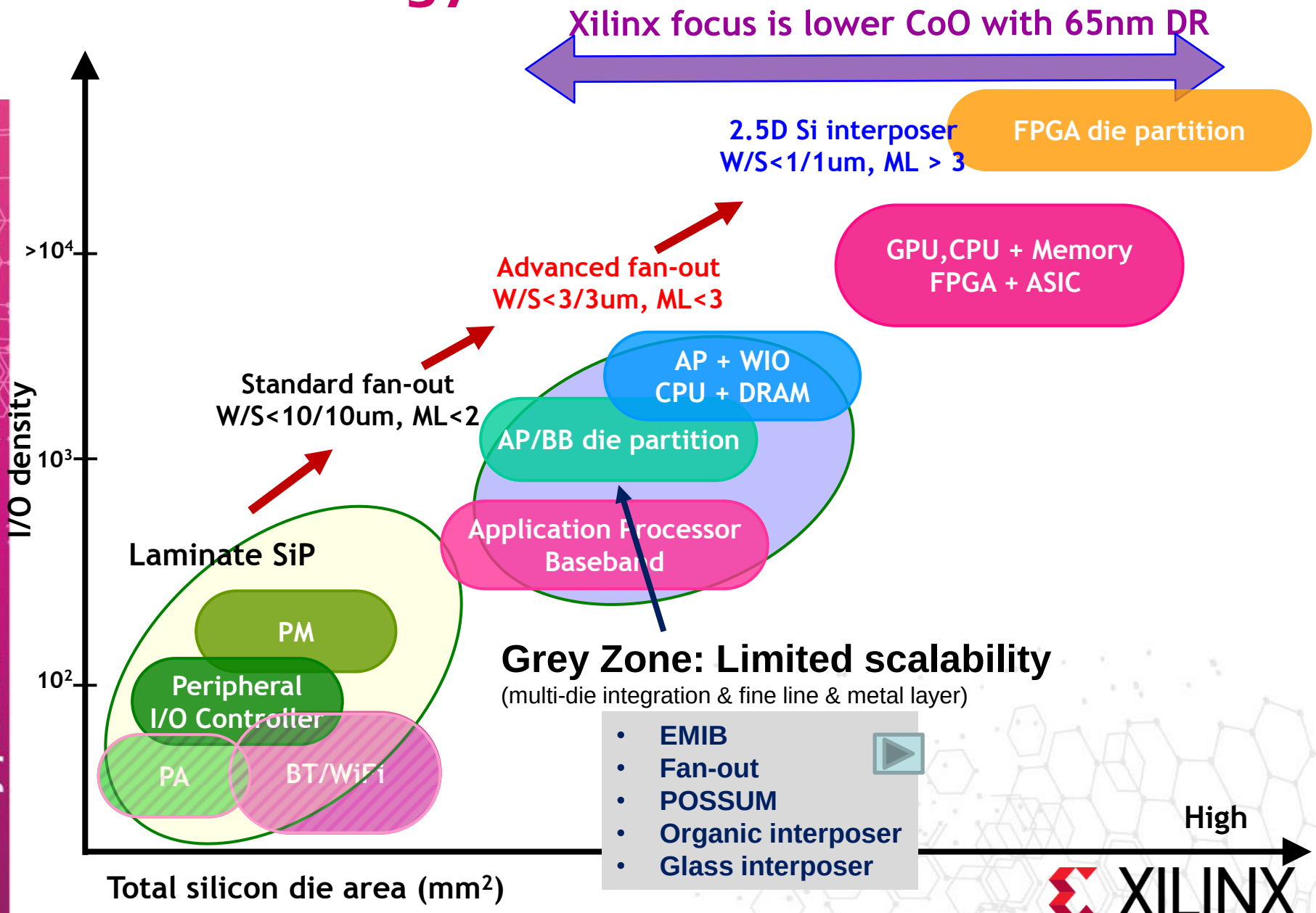
3DIC Extends Moore's Law

Cost Comparison: Monolithic vs. Multi-Die

"Moore's Law is Really About Economics" *– Gordon Moore*



2.5D Technology Platform



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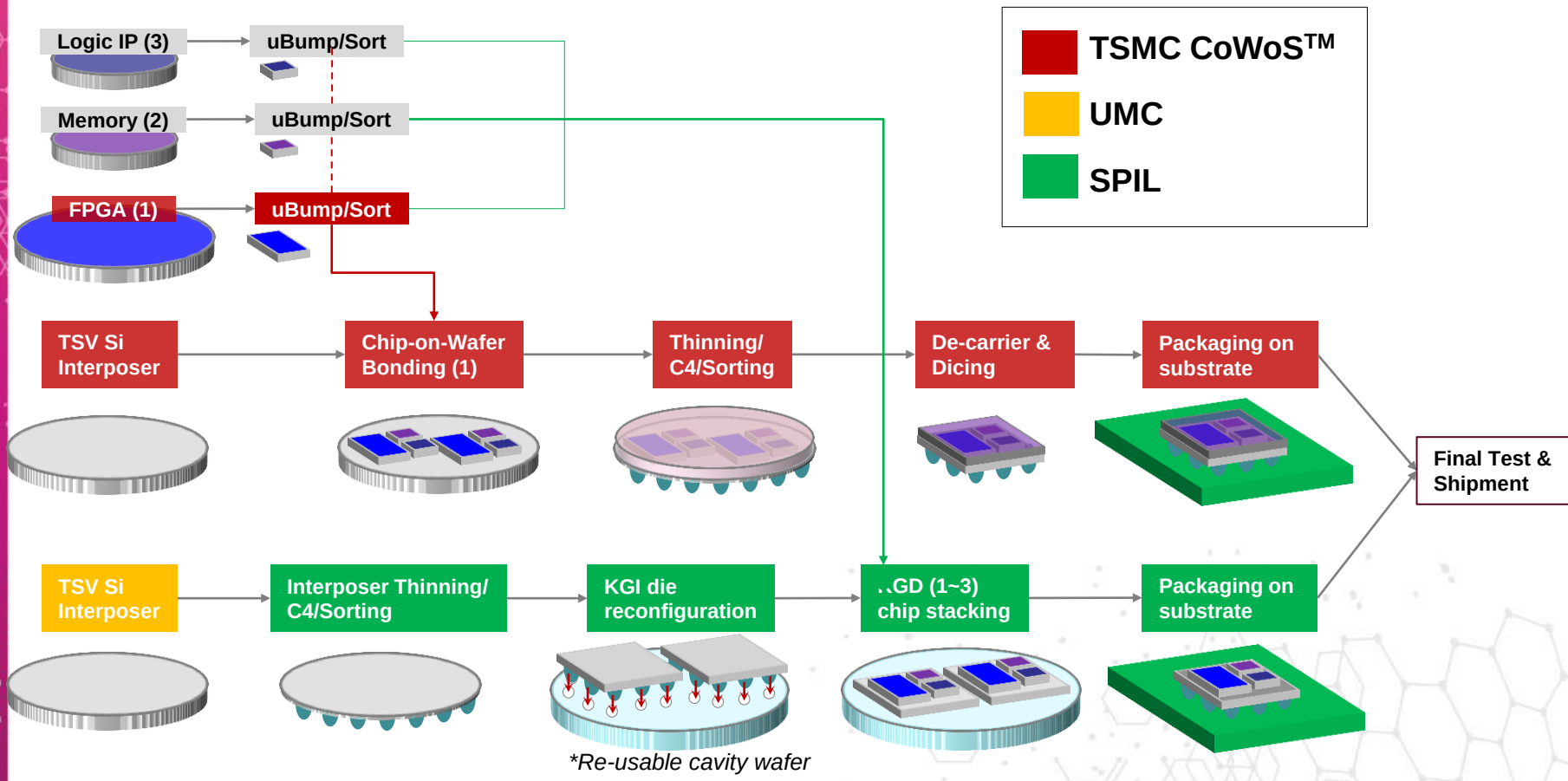
Supply Chain

- TSMC CoWoS in production
- UMC/SPIL technology is ready



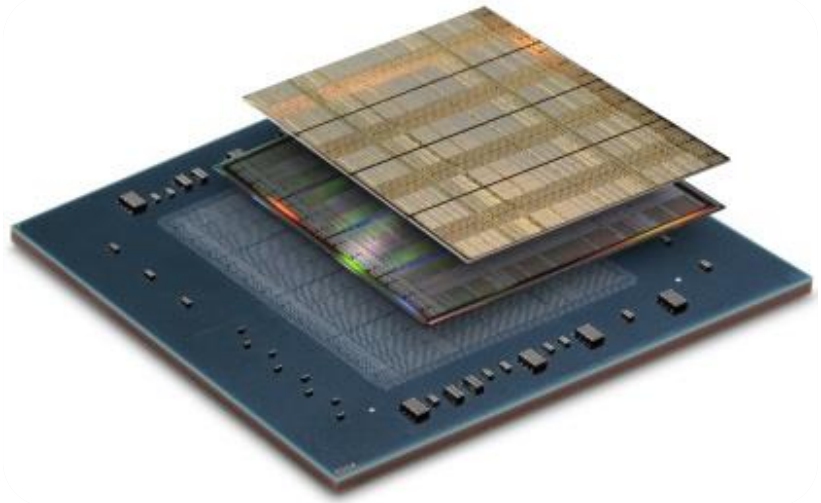
Xilinx 28nm 3D IC – Huge Leap in Innovation

Earth

Area: ~500 Million km²

Population: ~6.8 Billion People

Oceans: 5



Virtex-7 2000T

Interposer Area: ~775 mm²

Population: ~6.8 Billion Transistors

Chips: 5

- **136 Patents Awarded Worldwide**
- **226 Pending Applications Worldwide**

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3D IC Technology Development

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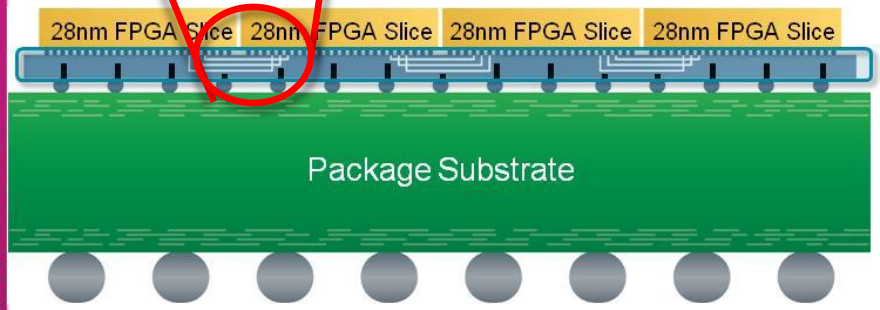
3D IC Anatomy & Assembly Flow

Passive Silicon Interposer (65nm)
- 4 Metal Layers Connecting Micro-Bumps & TSVs

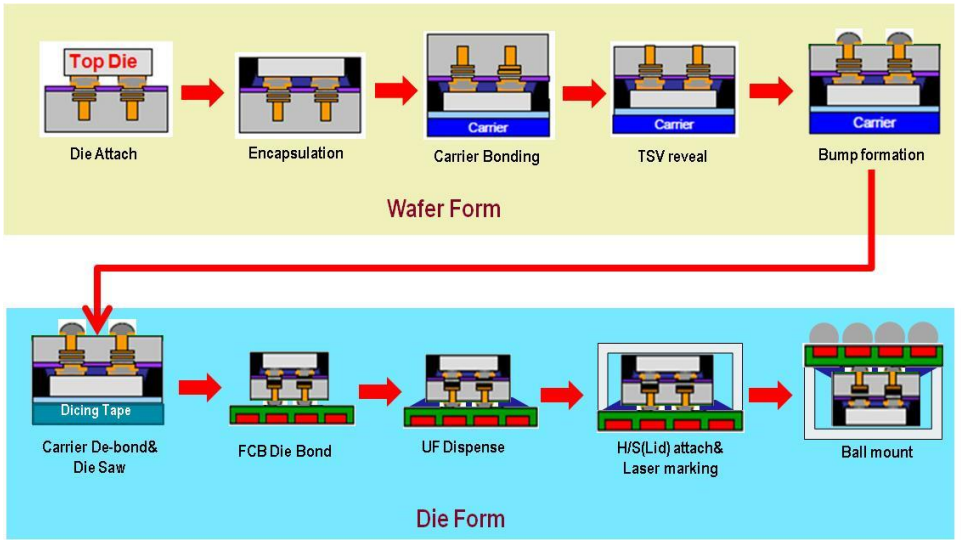
Micro-Bumps
- Power / Ground / IOs / Routing

C4 Bumps
- Connects Silicon to Package

Through-Silicon Via (TSVs)
- Connects Power / Ground / IOs to C4 Bumps



Primary Chip on Wafer Assembly Steps



- > 150,000 Micro-bumps
- > 10,000 TSVs
- > 10,000 C4 Bumps
- > 90 Processing Steps in 3D IC Flow (From Bump to Completed Package)

Achieved Good Yield & Quality

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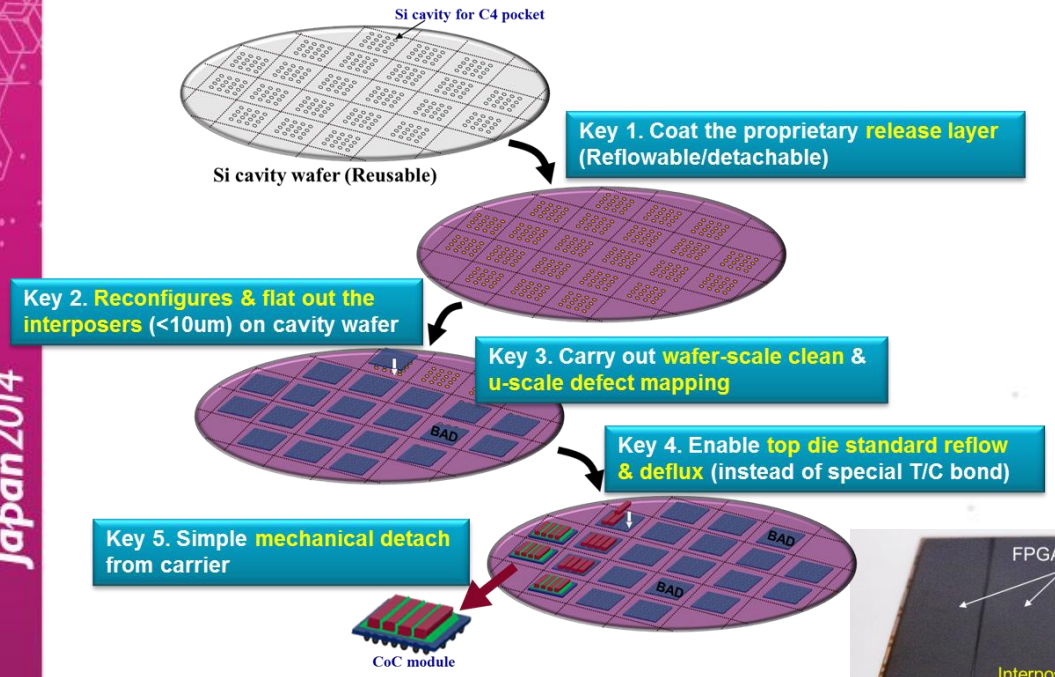
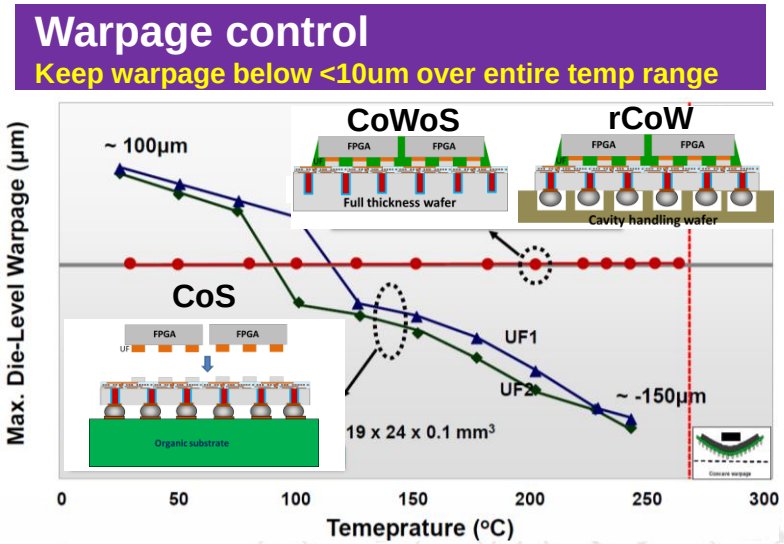
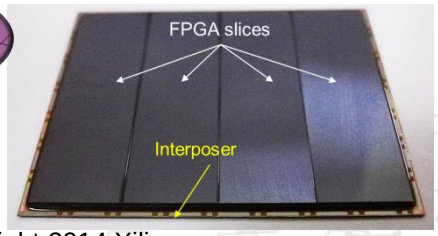
Critical Challenge: Warpage Control

- **CoWoS Technology**
  - Top dies are attached to full-thickness interposer wafers thus getting around the thin interposer warpage and poor micro-bump joining problem
- **Reconfigurable CoW (rCoW) Technology**
  - Xilinx patent issued worldwide (US/TWN/CN/EU/IND/JPN/KR)
  - Release layer approach that withstands reflow & maintains low warpage







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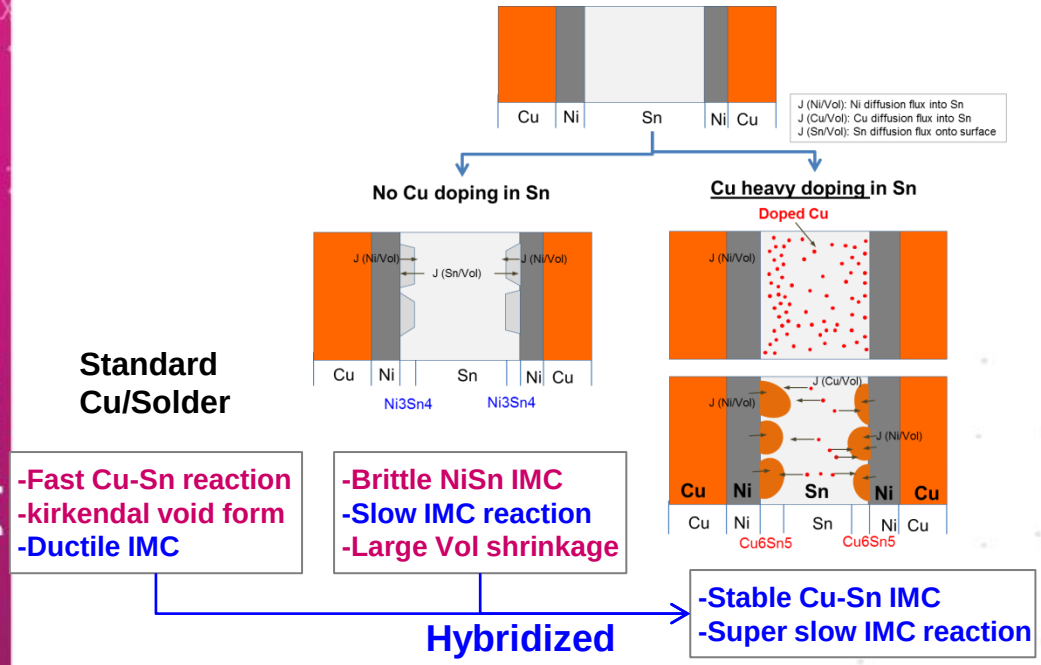
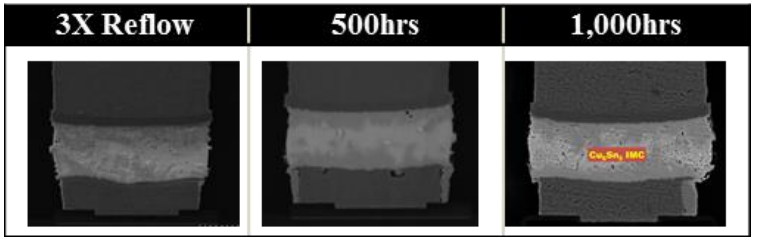
HTS Aging Reliability Issue

- **Voiding or crack in micro-joint during long term stress (HTS in particular)**
  - Due to limited Sn source and its dual consumption rate from top and bottom pad
- **Resolution : Heavy Cu doping into LF solder cap (with Ni barrier layer)**
  - Take advantages of ductile IMC (Cu-Sn) and slower IMC reaction (Ni with Cu-Sn IMC)
  - Passed 3X reflow + 150°C aging condition for > 1000 hrs

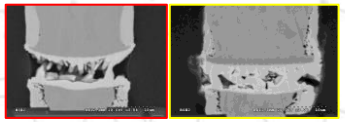
Diffusion flux model of inter-diffusion



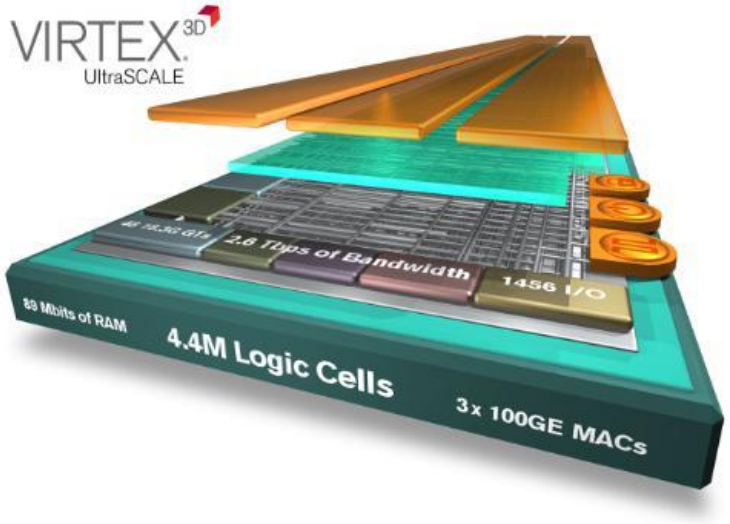
HTS aging performance



*Reference images
(from no-doping u-bump)

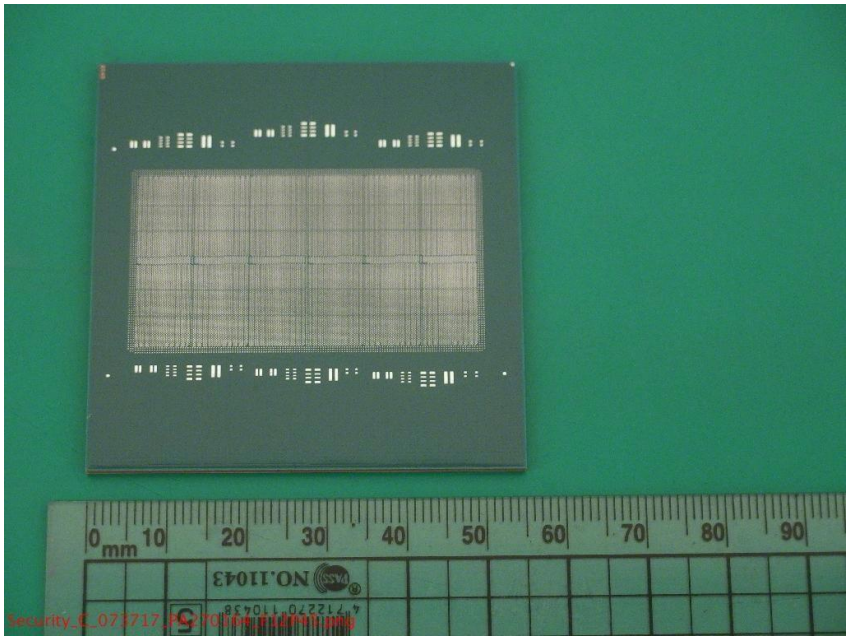


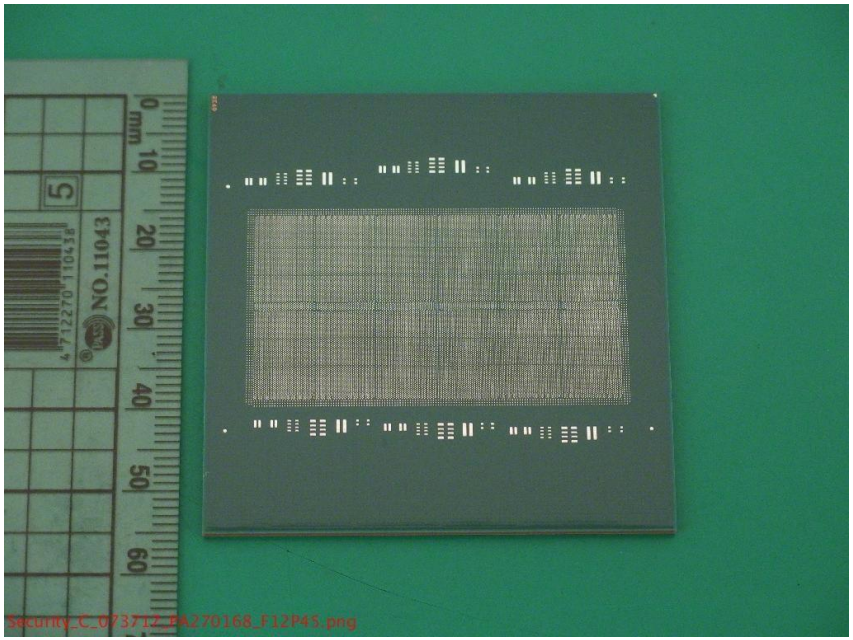
Leadership Continues at 20/16nm - UltraSCALE



- 4.4M Logic Cells in 20nm
- 14B transistors
- 600,000 micro-bumps
- 55mm package, 2892 pins

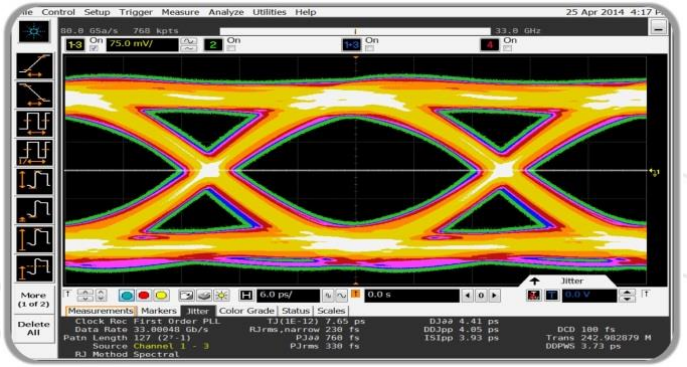
Leadership Continues at 20/16nm - UltraSCALE





- 2.0 dB insertion loss at Nyquist Frequency
- Low loss substrate and design
- 23,000 C4 bumps

32G TX Eye



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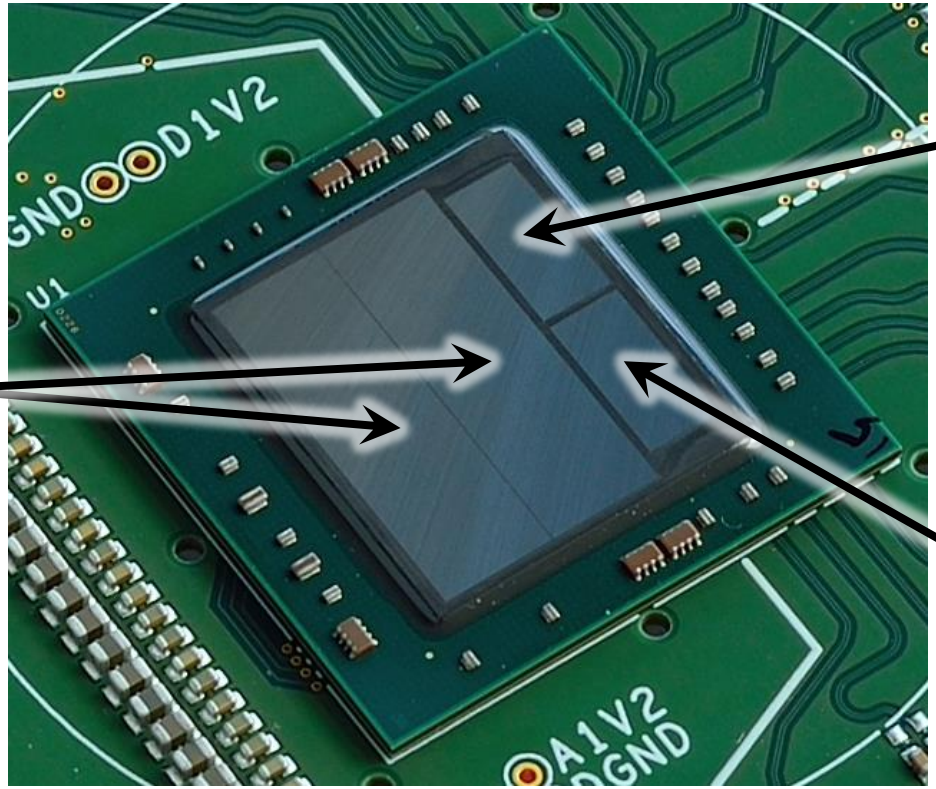
Demo High Performance Mixed Signal Integration



Array of 16 DACs
16-bit – 1.6GS/s

2 x Virtex-7
350T slices

Array of 16 ADCs
13-bit – 125MS/s

- **Industry first 3D FPGA/Mixed Signal integration (ISSCC 2014)**

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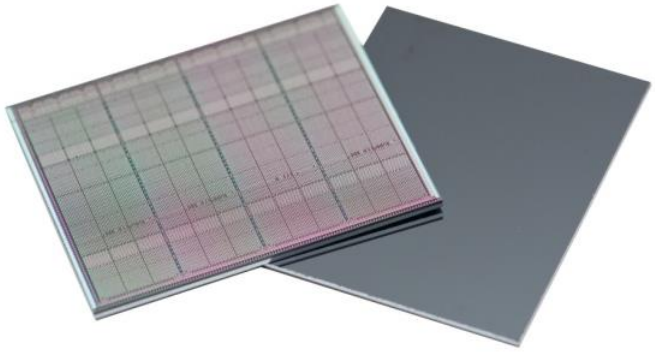
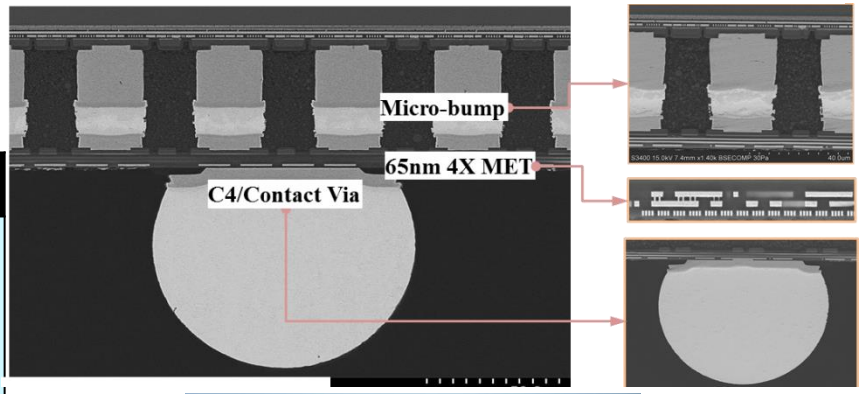
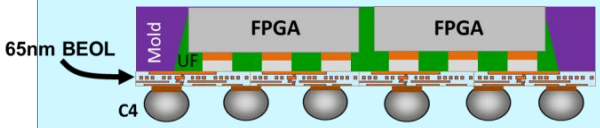
Si-Less/TSV-less Interconnect Tech (SLIT) Builds on Interposer

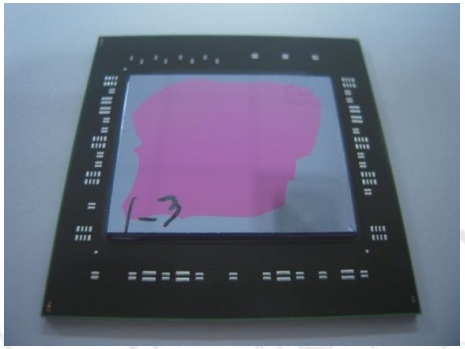


Key Benefits

- ***Lower cost of ownership***
  - No HR-Si substrate used & less process modules (No TSV module/TBDB/TSV revealing)



	SLIT (Under development)
Structure	
High-R Si substrate	×
65nm 4X Metal	○
TSV Creation	×
Micro-bumping	○
Temporary carrier	◎
Thinning	○
TSV Revealing	×



Xilinx, SPIL (iMAPS 2014)

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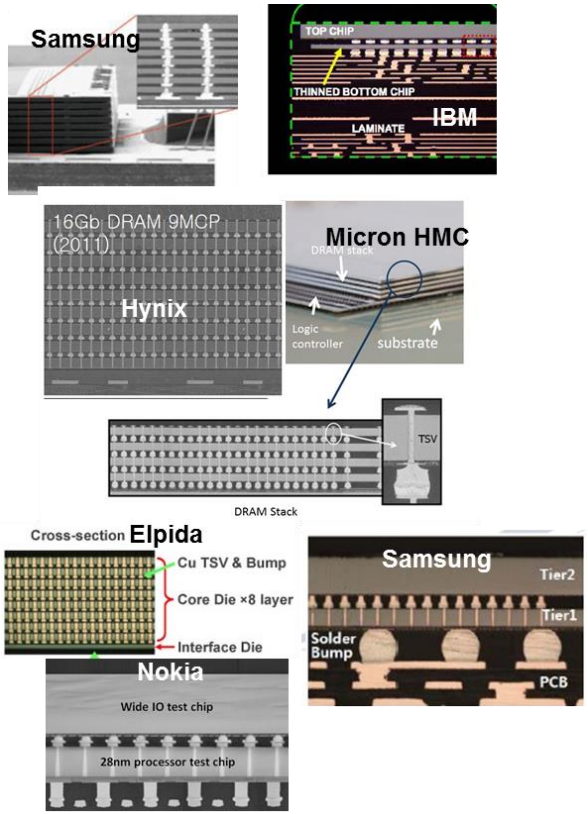
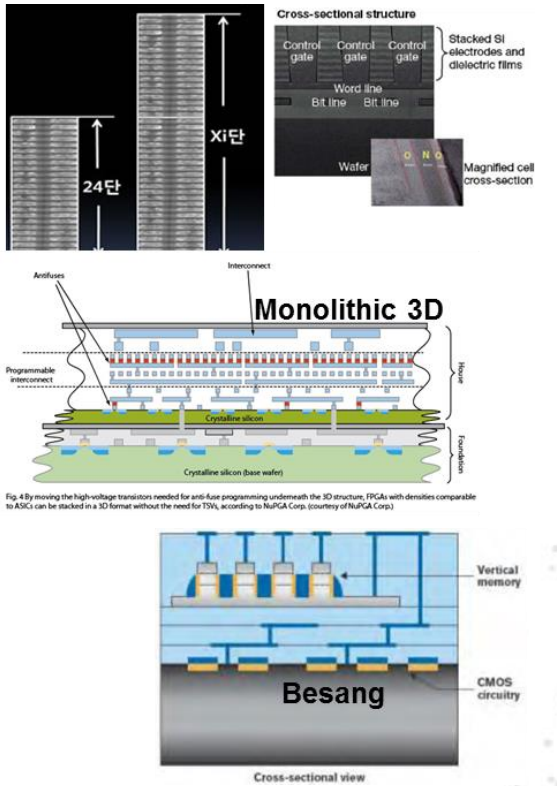
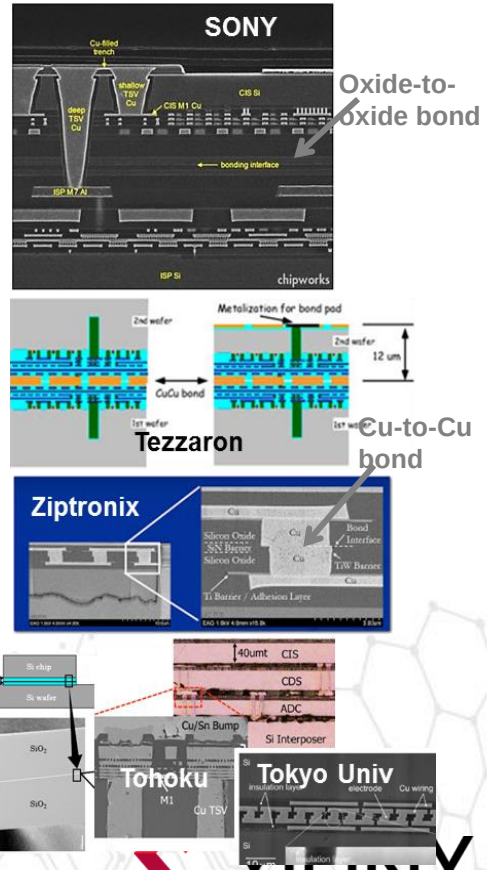
3D IC Technology Landscape

	Chip level	Device level	W2W C2W level
Players	**Samsung** DRAM / **Hynix** NAND & DRAM / **IBM** / **Micron** / **Elpida** / **Qualcomm** / **Nokia**	**Samsung** Vertical-Gate NAND/ **Besang** / Monolithic 3D IC / Stanford	**SONY (Stacked CIS)** / **Tezzaron** / Ziptronix/ MIT Lincon Lab
TSV size	5~10um	0.5~2um contact through oxide	2~5um in diameter
TSV pitch	30~50um	1~4um (not limited)	5~10um
TSV count	1k~5k	Not limited	Not limited
Key features			







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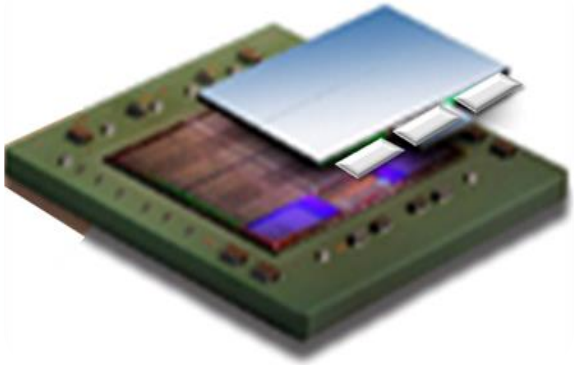
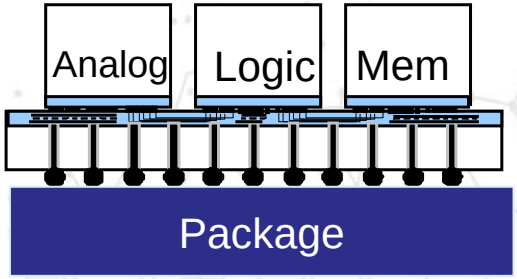
Summary

- Economic and technology forces are aligned to enable 2.5D/3D stacking

- TSV and 3D stacking already deployed in Smartphones, High end FPGAs & Servers



- The “end game” will see three distinct technologies: Logic, Memory, Analog



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Acknowledgements

- Xilinx
  - R&D, Reliability, NPI, Operations and Marketing Teams
- Partners
  - TSMC R&D and Production Teams for FPGA, CoWoS
  - UMC for Interposer
  - SPIL R&D for MEOL and Advanced Packaging
  - Fujitsu Interconnect Technology for High Speed Substrates

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Design Rule Comparison

Design Rules for Die to Die interconnection	MCM (Substrate)	EMIB	Silicon Interposer (65 nm BEOL)	WLFO / Organic Interposer
Minimum Bump pitch (um)	150 (C4)	150 (C4) 40 (u-bump) bridge	< 40 (u-bump)	40 um RDL pad pitch
Via size / pad size (um)	60 / 90	0.4 / 0.7	0.4 / 0.7	10/30
Minimum Line & Space (um)	15 / 15	0.4 / 0.4	0.4 / 0.4	3 / 3
Metal thickness (um)	10	1	1	2-5
Dielectric thickness (um)	30	1	1	< 5
# of die-to-die connections per layer + GND shield layer (2L)	100's	10,000's	10,000's	1000's
Minimum die to die spacing (um)	4000	Bridge ~ 2500	150	< 250
# of High density layers feasible	Not a limitation	Not a limitation	Not a limitation	1-3L layers
Die Sizes for assembly and # of assemblies	Not a concern	Size & # limitation?	Not a concern	Size limitation?

- **Xilinx pursuing Silicon Interposer for design rule density, BW and lower power – e.g. die partition**